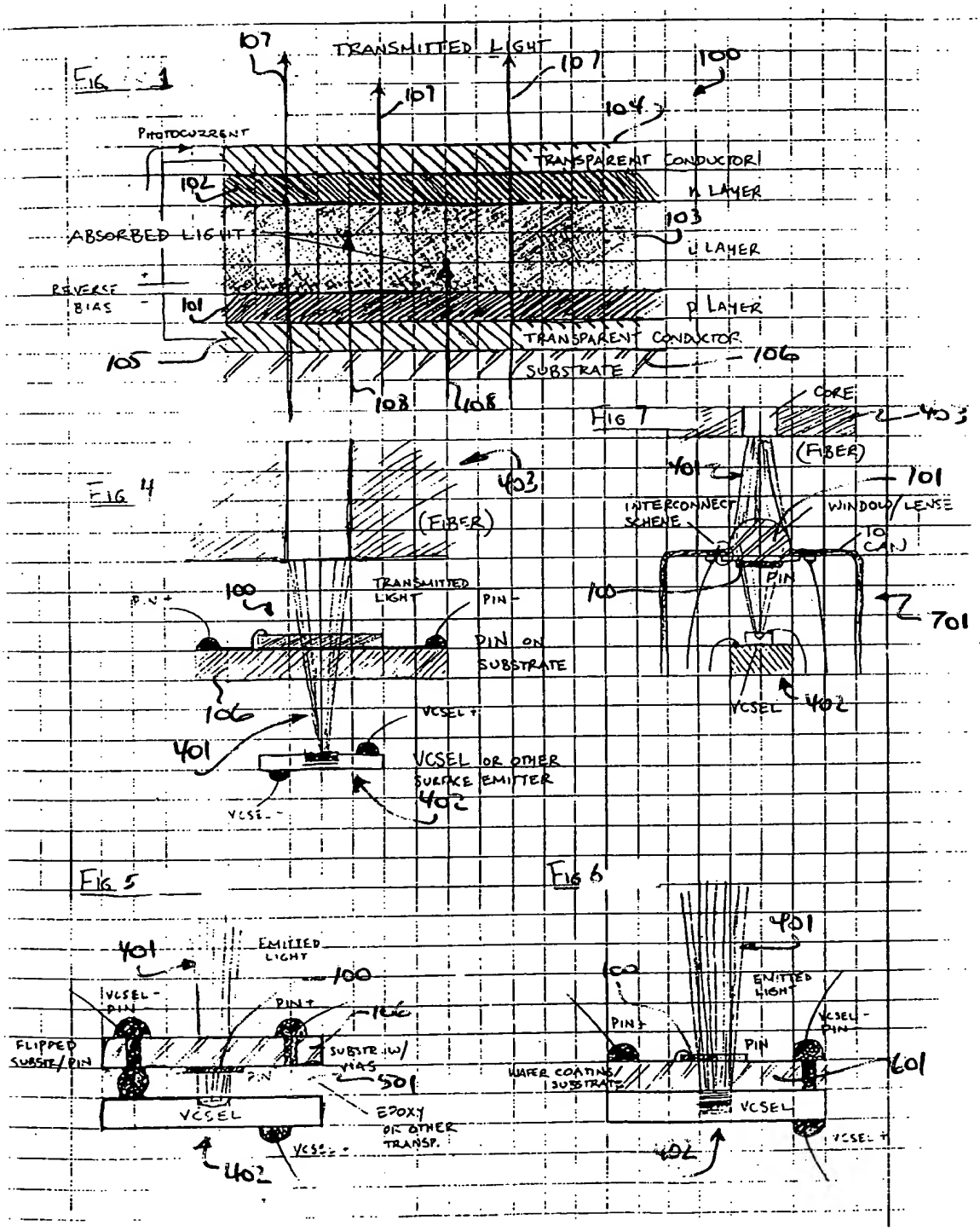


FIG 1
TRANSMITTED LIGHT
107
107
107
100
104
PHOTOCURRENT
TRANSPARENT CONDUCTOR
102
n LAYER
ABSORBED LIGHT
103
i LAYER
REVERSE BIAS
101
p LAYER
TRANSPARENT CONDUCTOR
105
SUBSTRATE
106
103
108
FIG 4
403
(FIBER)
TRANSMITTED LIGHT
PIN +
PIN -
100
PIN ON SUBSTRATE
106
VCSEL +
401
VCSEL OR OTHER SURFACE EMITTER
402
VCSEL -
FIG 7
CORE
403
(FIBER)
401
101
INTERCONNECT SCHEME
WINDOW/LENSE
TO CAN
PIN
100
701
VCSEL
402
FIG 5
401
EMITTED LIGHT
100
VCSEL - PIN
PIN +
106
FLIPPED SUBSTR/PIN
SUBSTR. W/ VIAS
501
PIN
VCSEL
EPOXY OR OTHER TRANSP.
VCSEL -
402
FIG 6
401
100
EMITTED LIGHT
PIN +
VCSEL - PIN
PIN
WAFER COATING/ SUBSTRATE
601
VCSEL
402
VCSEL +

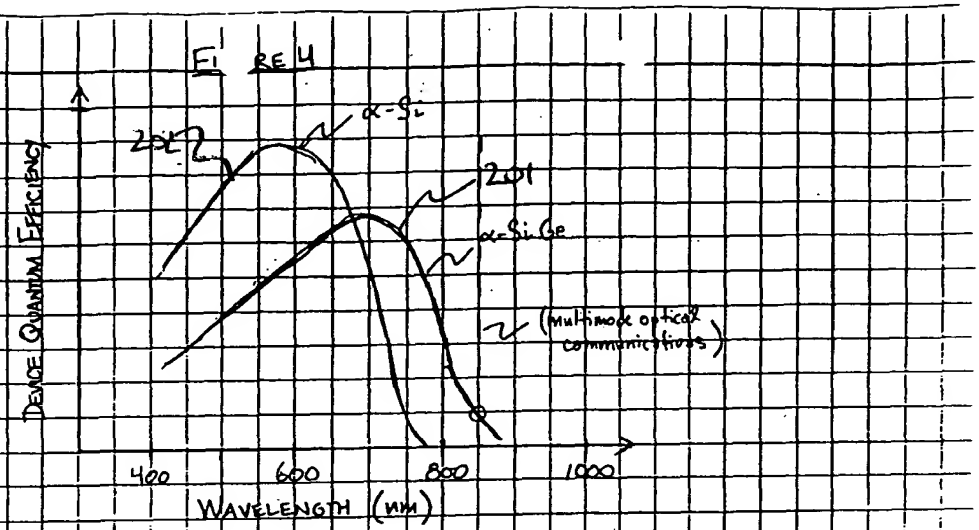

FIRE 4
DEVICE QUANTUM EFFICIENCY
202
α-Si
201
α-Si Ge
(multimode optical communications)
400
600
800
1000
WAVELENGTH (nm)

Fig. 2

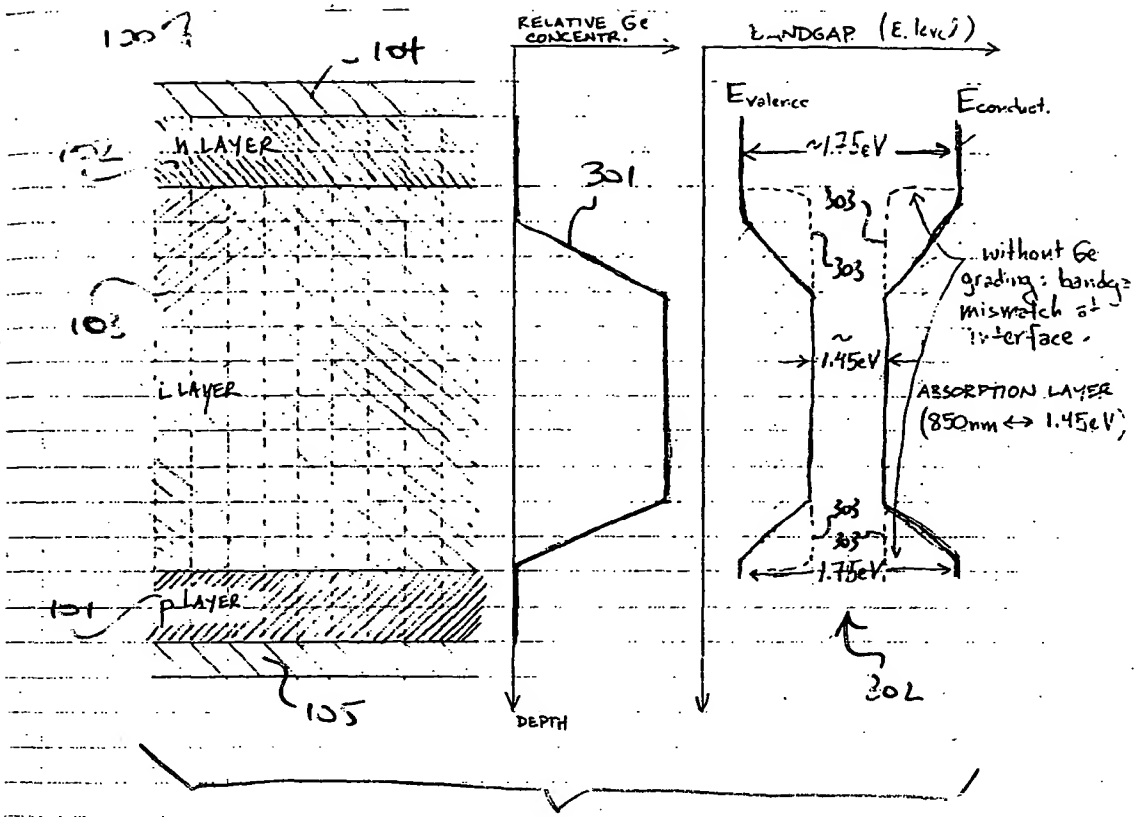

100
104
N LAYER
102
301
103
I LAYER
P LAYER
101
105
RELATIVE Ge CONCENTR.
DEPTH
BANDGAP (E. level)
E valence
E conduct.
~1.75eV
303
303
without Ge grading: bandgap mismatch at interface.
~1.45eV
ABSORPTION LAYER (850nm ↔ 1.45eV)
303
303
1.75eV
202

Fig. 3

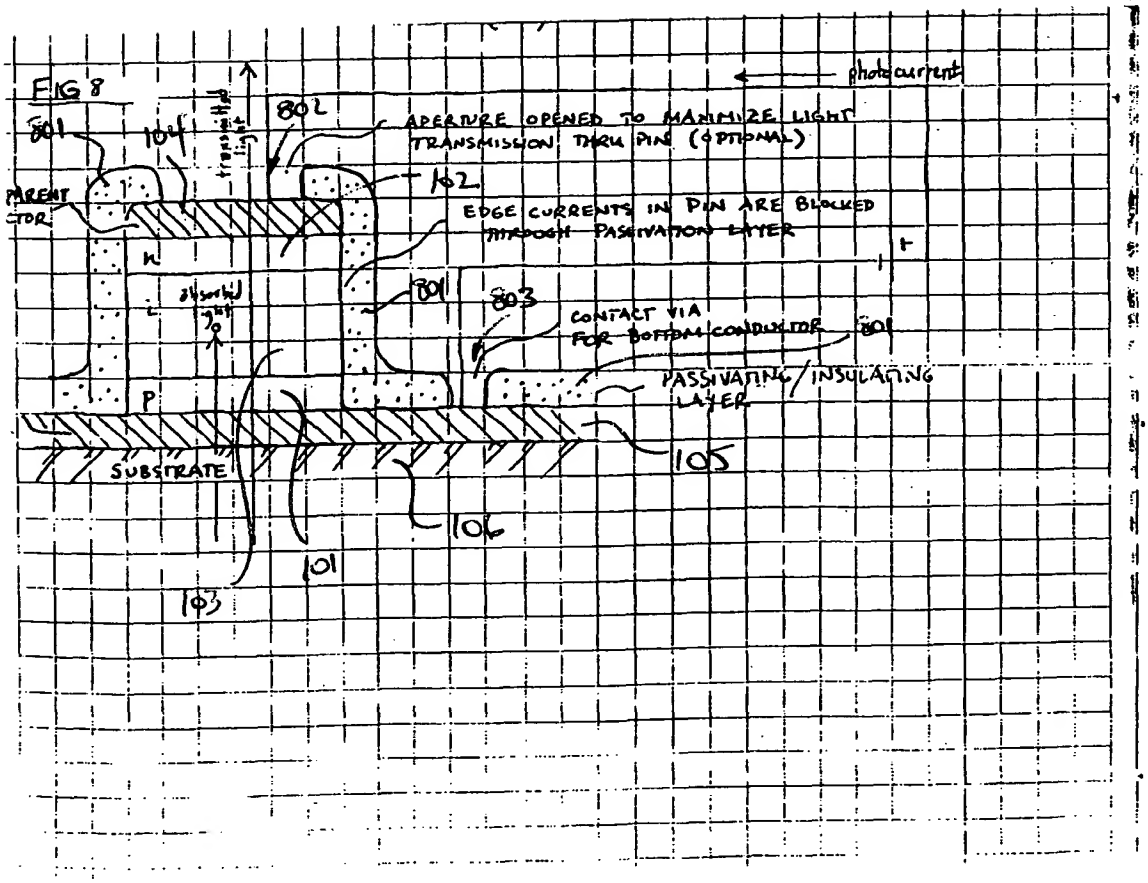


FIG 8
801
104
802
APERATURE OPENED TO MAXIMIZE LIGHT TRANSMISSION THRU PIN (OPTIONAL)
102
EDGE CURRENTS IN PIN ARE BLOCKED THROUGH PASSIVATION LAYER
803
CONTACT VIA FOR BOTTOM CONDUCTOR
PASSIVATING/INSULATING LAYER
105
SUBSTRATE
106
101
103
N
P
I
photocurrent

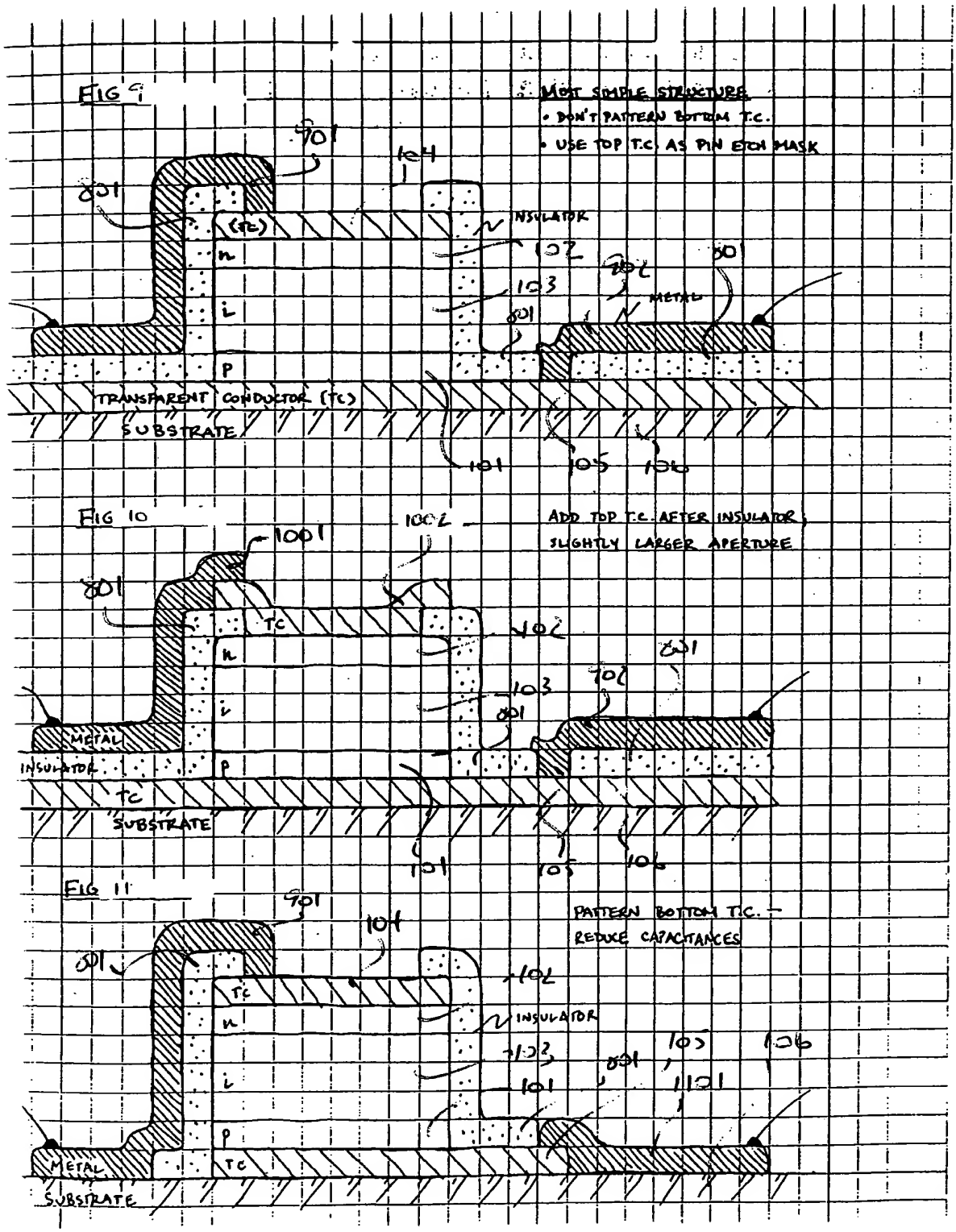


FIG 9
MOST SIMPLE STRUCTURE
• DON'T PATTERN BOTTOM T.C.
• USE TOP T.C. AS PIN ETCH MASK
901
104
801
(TC)
n
i
P
INSULATOR
102
103
102
901
METAL
TRANSPARENT CONDUCTOR (TC)
SUBSTRATE
101
105
106
FIG 10
ADD TOP T.C. AFTER INSULATOR;
SLIGHTLY LARGER APERTURE
1001
1002
801
TC
n
i
P
METAL
INSULATOR
TC
SUBSTRATE
101
105
106
FIG 11
PATTERN BOTTOM T.C. —
REDUCE CAPACITANCES
901
104
801
TC
n
i
P
TC
METAL
SUBSTRATE
102
INSULATOR
103
101
105
106
1101

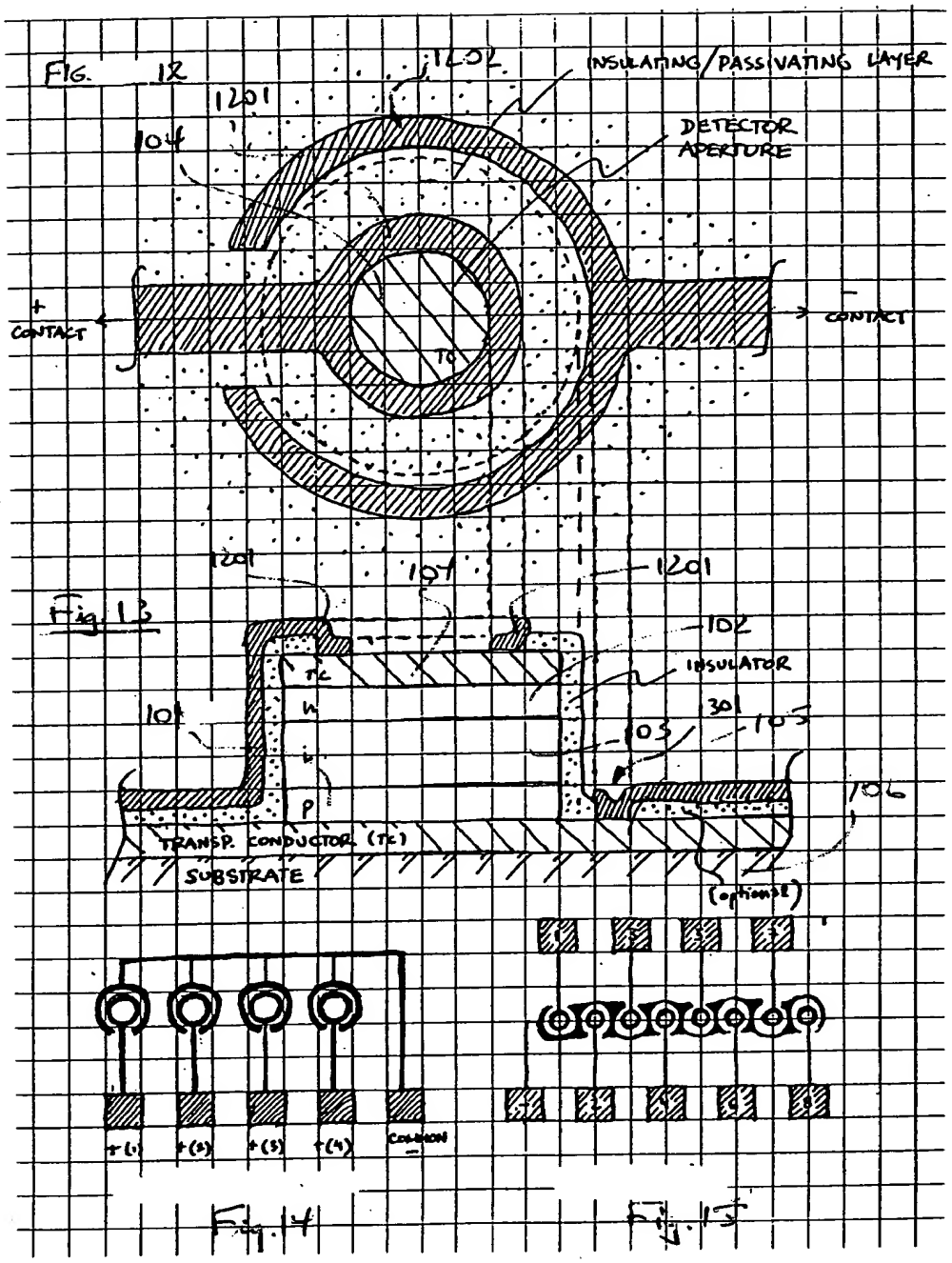


FIG. 12
1201
INSULATING/PASSIVATING LAYER
104
DETECTOR APERTURE
+ CONTACT
- CONTACT
Fig 13
1201
101
1201
102
INSULATOR
TC
W
301
101
105
105
t
106
P
TRANSP. CONDUCTOR (TC)
SUBSTRATE
(optional)
+(1)
+(2)
+(3)
+(4)
COMMON
Fig. 14
Fig. 15

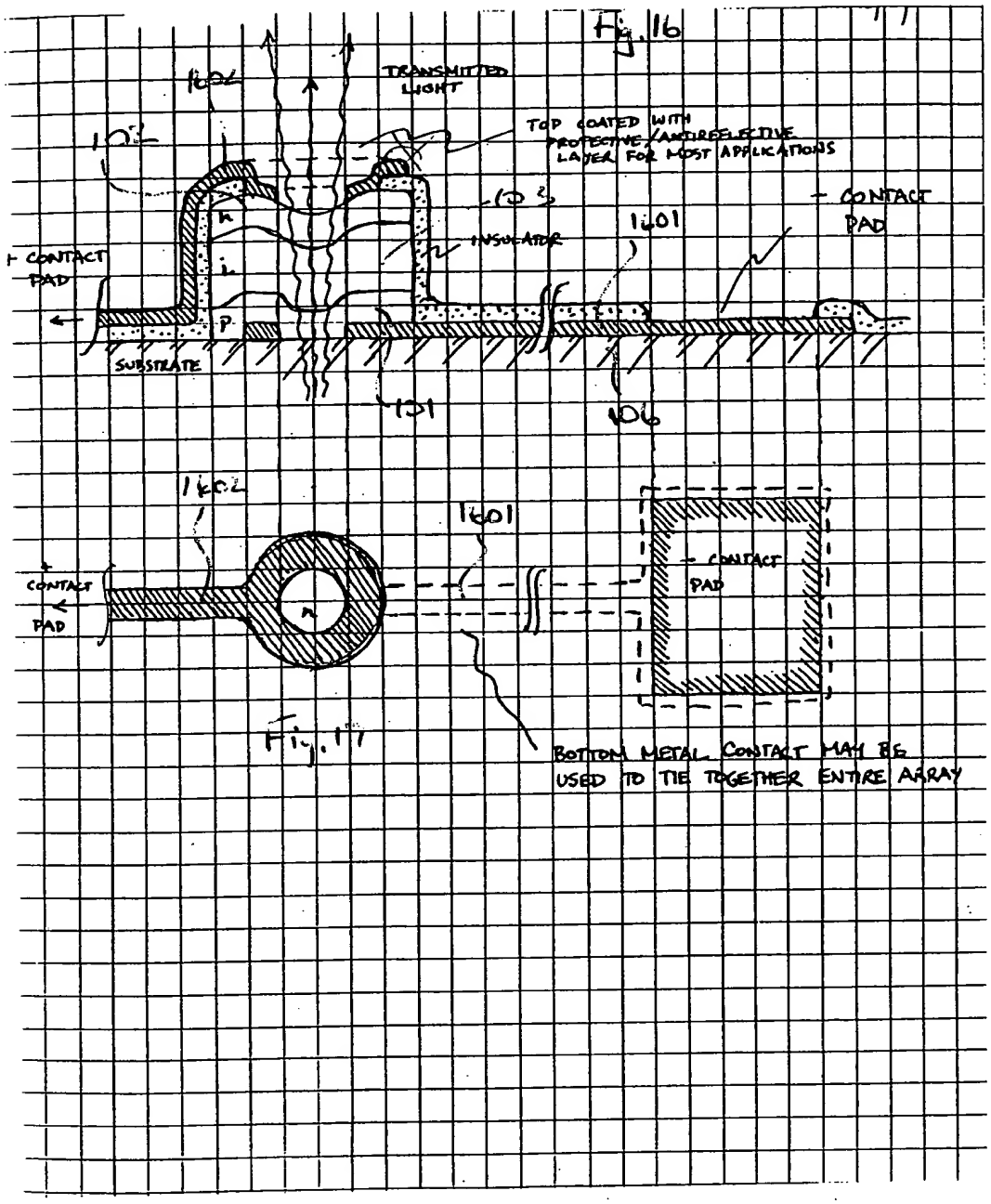
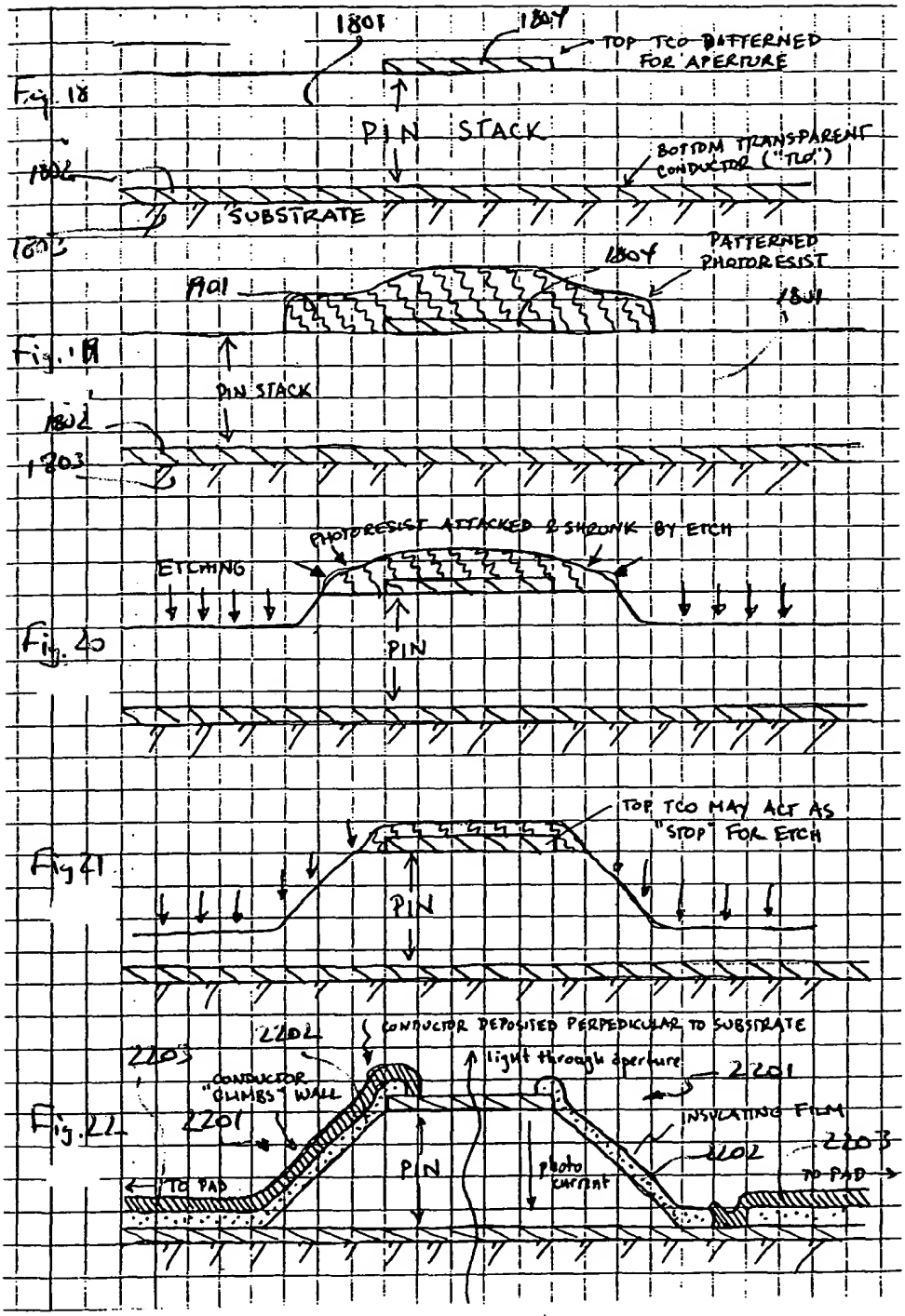


Fig. 16
TRANSMITTED LIGHT
TOP COATED WITH PROTECTIVE/ANTIREFLECTIVE LAYER FOR MOST APPLICATIONS
+ CONTACT PAD
INSULATOR
+ CONTACT PAD
SUBSTRATE
Fig. 17
+ CONTACT PAD
BOTTOM METAL CONTACT MAY BE USED TO TIE TOGETHER ENTIRE ARRAY


1801
1804
TOP TCO PATTERNED FOR APERTURE
Fig. 18
PIN STACK
1802
BOTTOM TRANSPARENT CONDUCTOR ("TCO")
SUBSTRATE
1803
1804
PATTERNED PHOTORESIST
1801
Fig. 1B
PIN STACK
1802
1803
PHOTORESIST ATTACKED & SHRUNK BY ETCH
ETCHING
Fig. 40
PIN
TOP TCO MAY ACT AS "STOP" FOR ETCH
Fig 41
PIN
CONDUCTOR DEPOSITED PERPENDICULAR TO SUBSTRATE
2202
2203
light through aperture
2201
"CONDUCTOR CLIMBS" WALL
2201
INSULATING FILM
2202
2203
Fig. 22
PIN
photo current
TO PAD
TO PAD

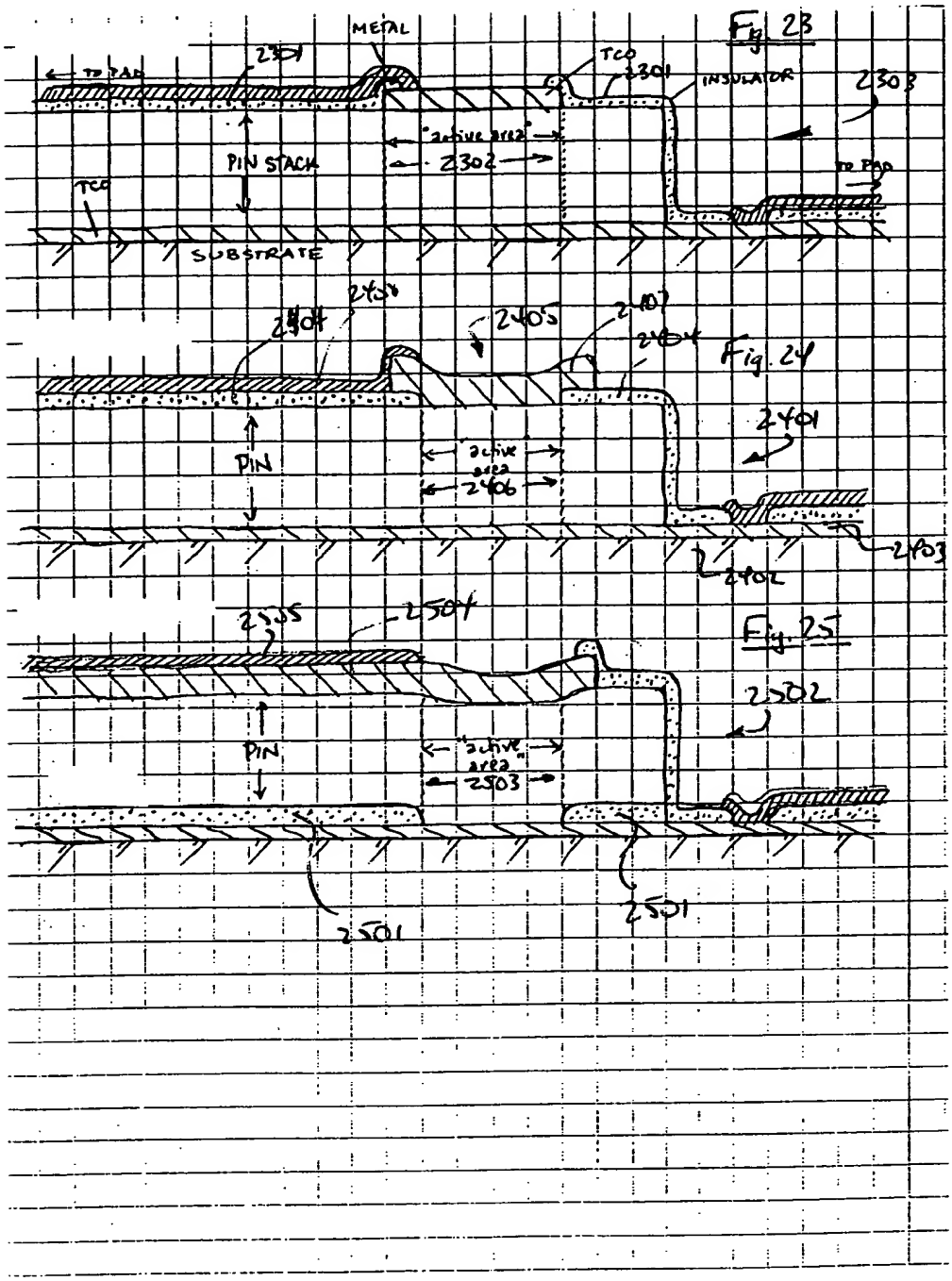
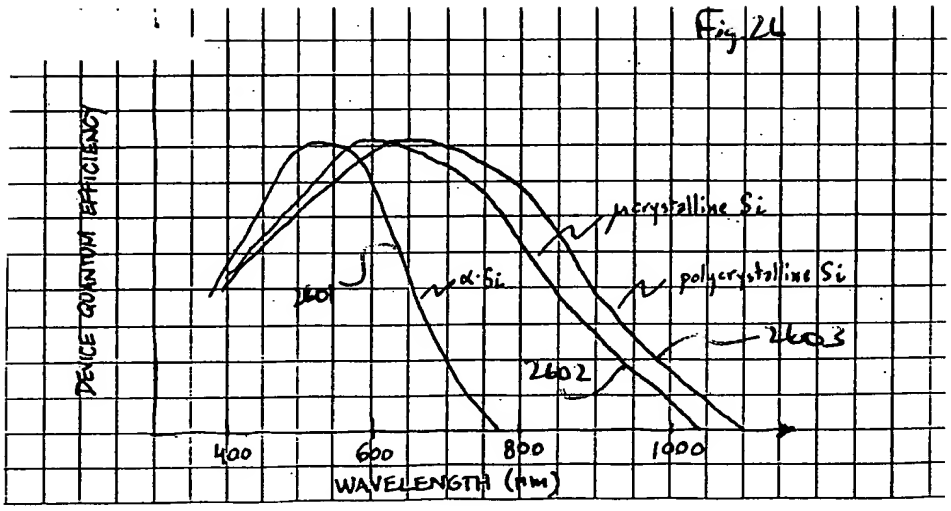


Fig 23
METAL
2301
TO PAD
TCO
2301
INSULATOR
2303
"active area"
2302
PIN STACK
TCO
SUBSTRATE
TO PAD
2404
2405
2407
2404
Fig. 24
2401
PIN
active area
2406
2403
2402
2505
2504
Fig. 25
2502
PIN
active area
2503
2501
2501

Fig 26


DEVICE QUANTUM EFFICIENCY
400
600
800
1000
WAVELENGTH (nm)
2601
a-Si
microcrystalline Si
polycrystalline Si
2602
2603

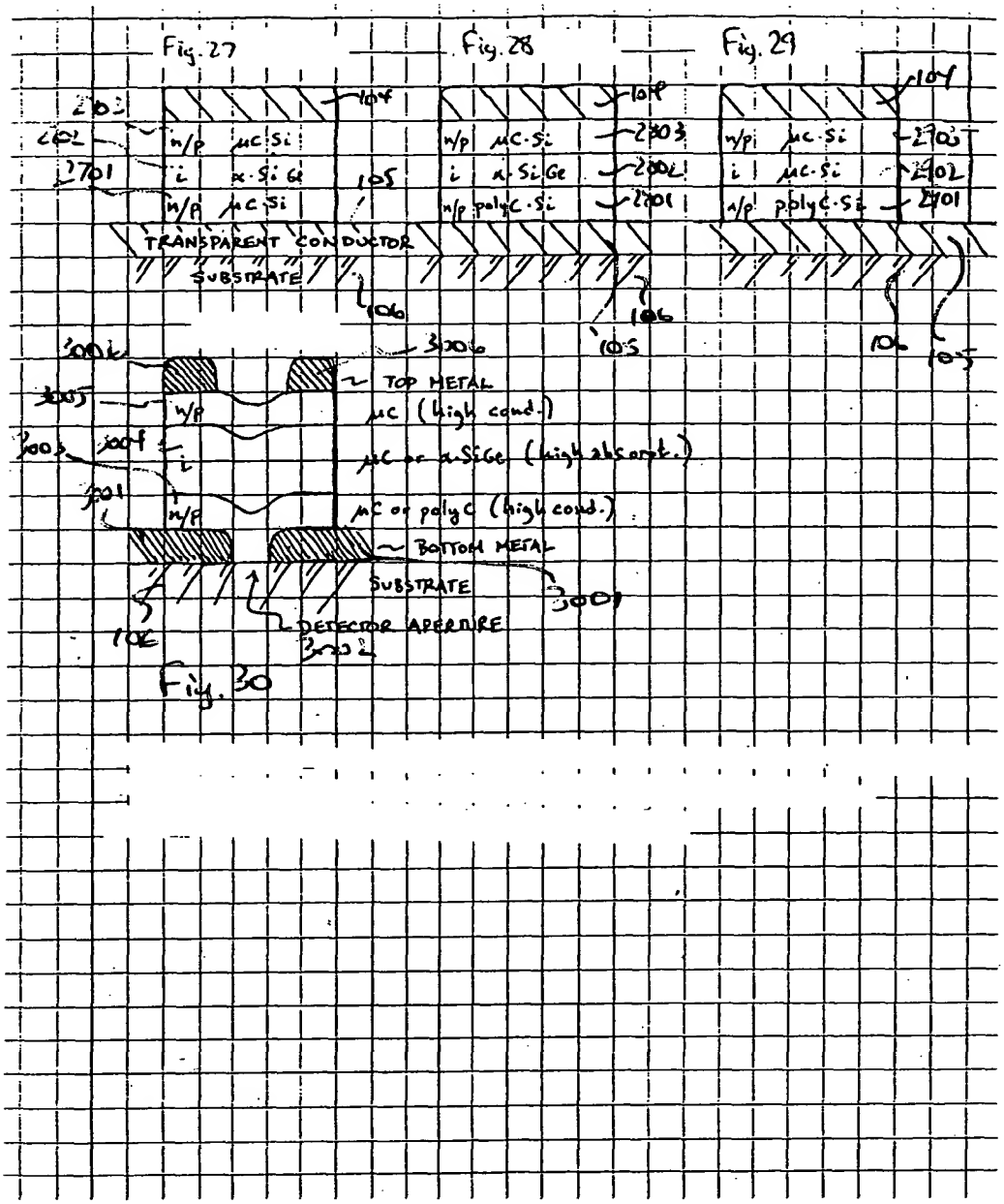


Fig. 27
Fig. 28
Fig. 29
TRANSPARENT CONDUCTOR
SUBSTRATE
TOP METAL
μc (high cond.)
μC or a-SiGe (high absorpt.)
μC or polyC (high cond.)
BOTTOM METAL
SUBSTRATE
DETECTOR APERTURE
Fig. 30

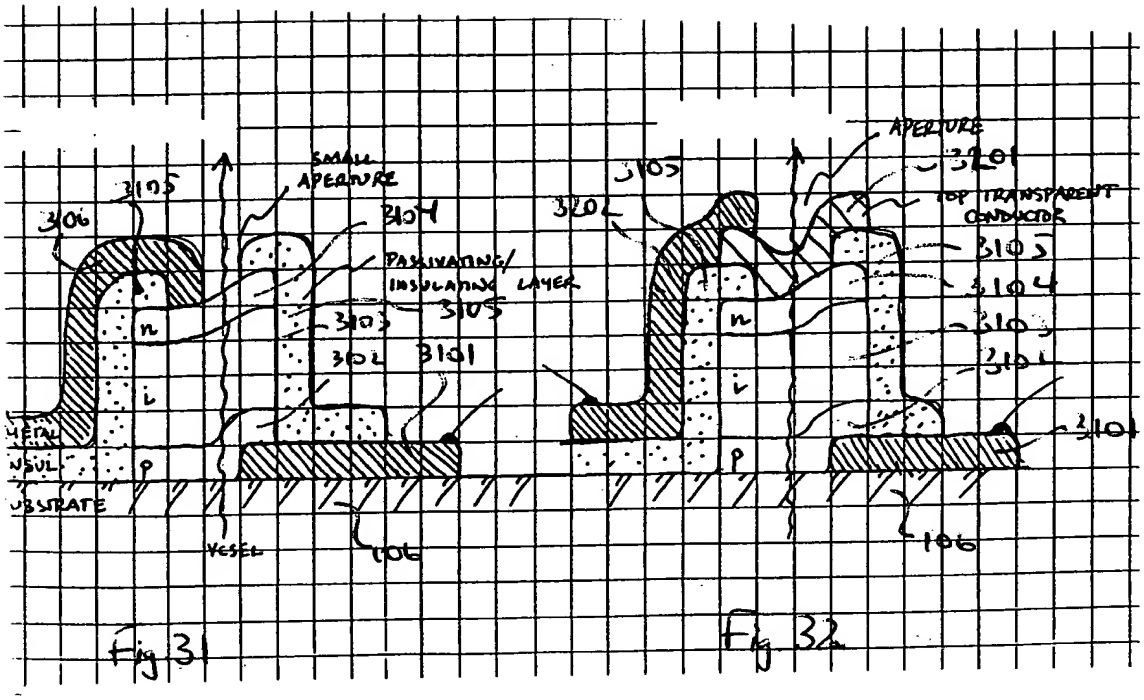

3105
3106
SMALL APERTURE
3104
PASSIVATING/ INSULATING LAYER
3103
3102
3101
n
i
p
METAL
INSUL
SUBSTRATE
VESEL
106
3105
APERTURE
3101
TOP TRANSPARENT CONDUCTOR
3103
3104
3102
3101
n
i
p
3101
106

Fig 31

Fig 32

09813454.032001

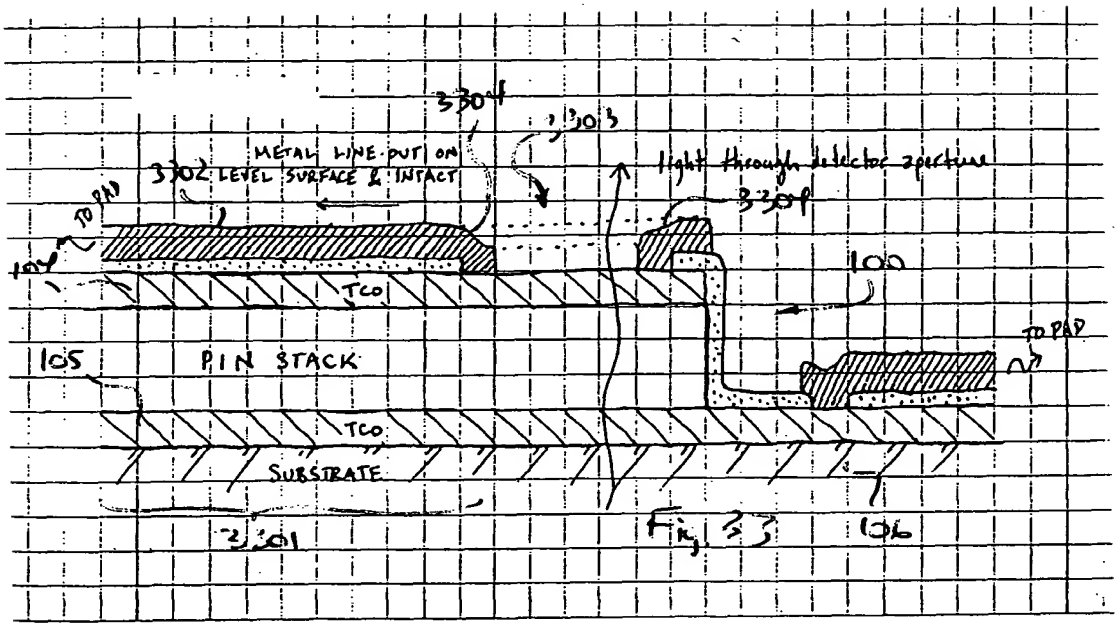


Fig. 3

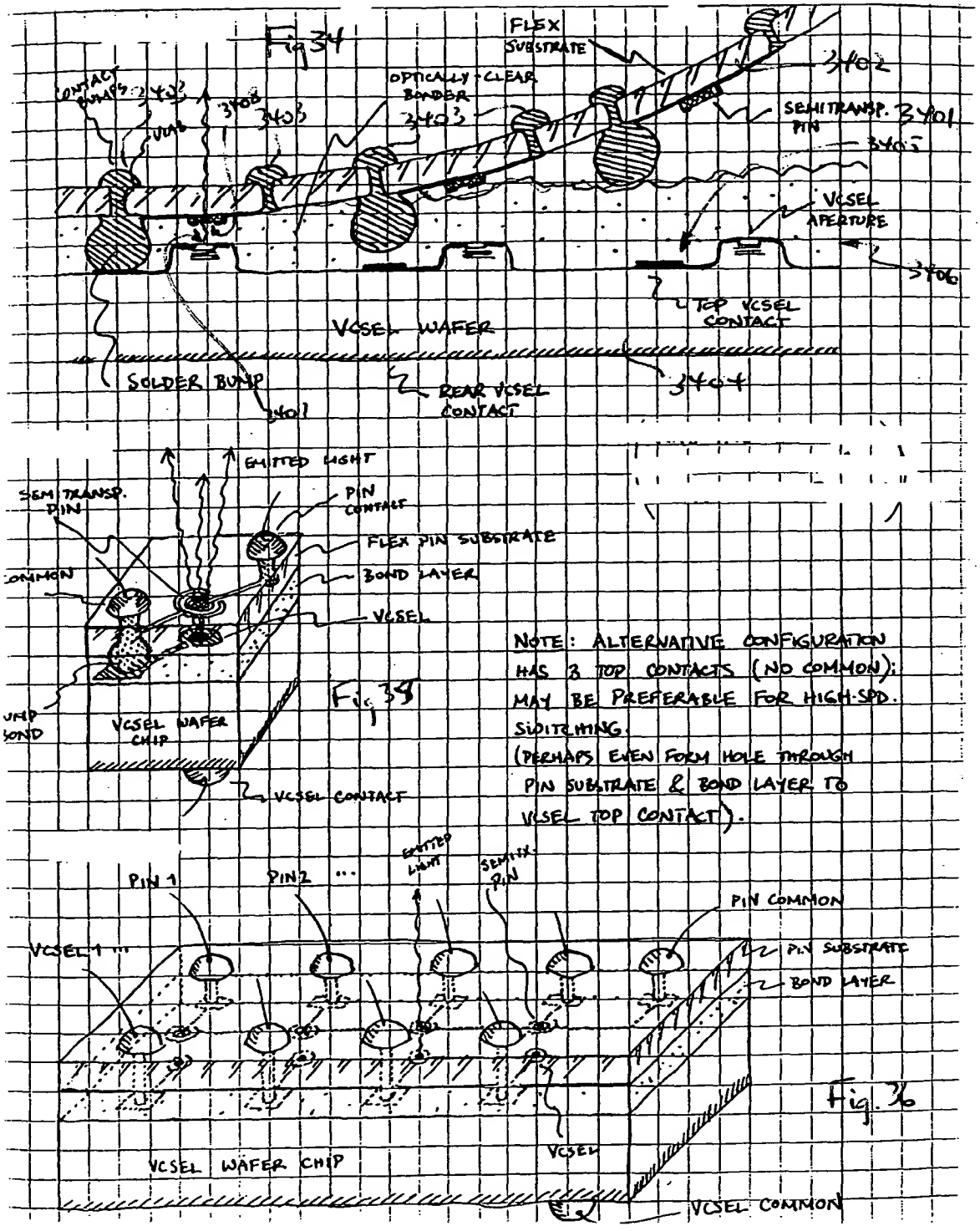


Fig 34
FLEX SUBSTRATE
3402
OPTICALLY CLEAR BONDER
3403
SEMITRANSP. PIN
3401
3405
VCSEL APERTURE
3406
TOP VCSEL CONTACT
VCSEL WAFER
3404
SOLDER BUMP
3401
REAR VCSEL CONTACT
EMITTED LIGHT
SEM TRANSP. PIN
PIN CONTACT
FLEX PIN SUBSTRATE
BOND LAYER
VCSEL
VCSEL WAFER CHIP
VCSEL CONTACT
Fig 35
NOTE: ALTERNATIVE CONFIGURATION HAS 3 TOP CONTACTS (NO COMMON); MAY BE PREFERABLE FOR HIGH-SPD. SWITCHING.
(PERHAPS EVEN FORM HOLE THROUGH PIN SUBSTRATE & BOND LAYER TO VCSEL TOP CONTACT).
PIN 1
PIN 2
EMITTED LIGHT
PIN COMMON
PIN SUBSTRATE
BOND LAYER
VCSEL 1
VCSEL WAFER CHIP
VCSEL
VCSEL COMMON
Fig. 36

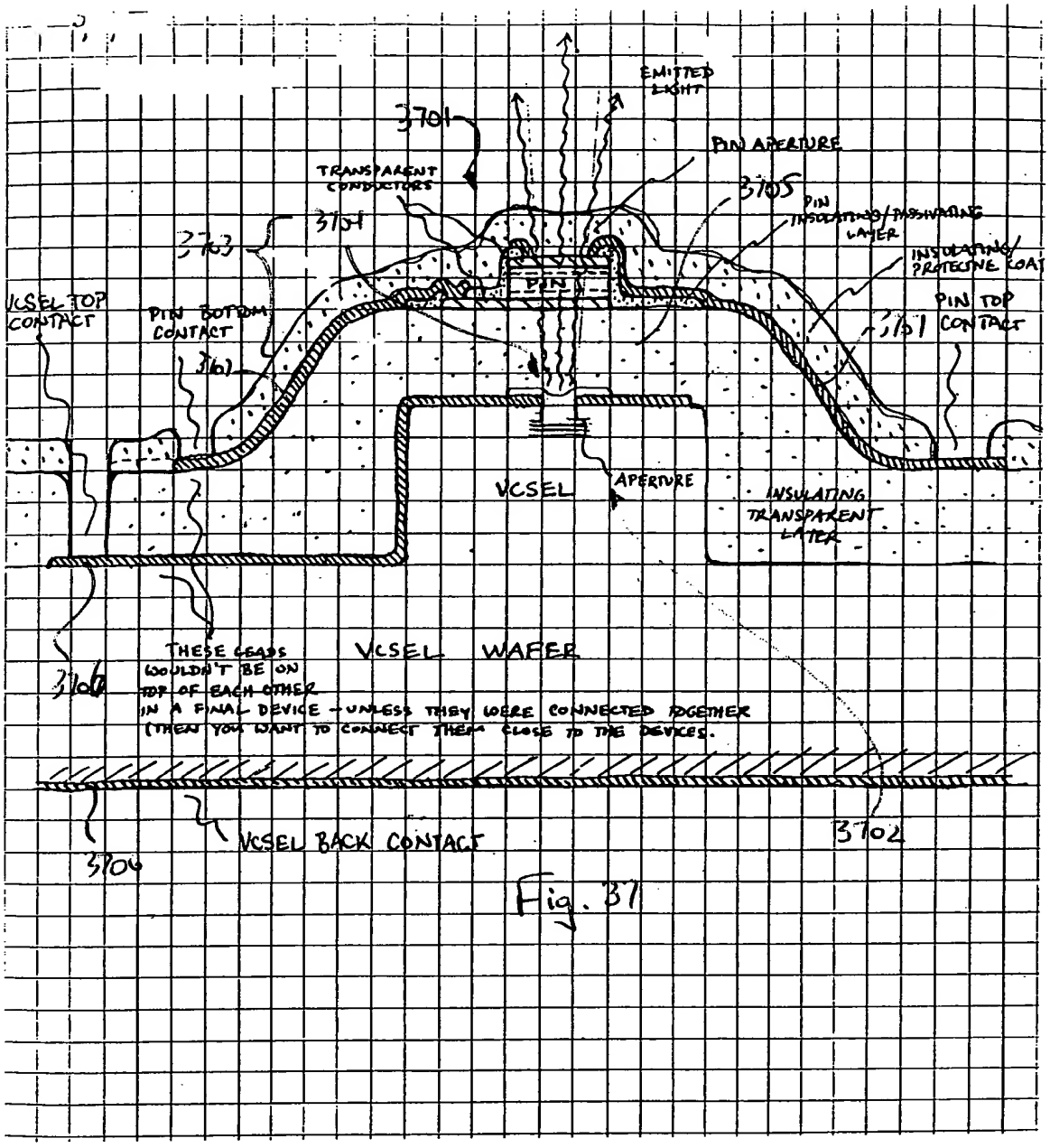

EMITTED LIGHT
3701
PIN APERTURE
TRANSPARENT CONDUCTORS
3705
PIN INSULATING/PASSIVATING LAYER
3703
3704
INSULATING/PROTECTIVE COAT
PIN
VCSEL TOP CONTACT
PIN BOTTOM CONTACT
3707
PIN TOP CONTACT
VCSEL
APERTURE
INSULATING TRANSPARENT LAYER
VCSEL WAFER
3706
THESE LEADS WOULDN'T BE ON TOP OF EACH OTHER IN A FINAL DEVICE - UNLESS THEY WERE CONNECTED TOGETHER (THEN YOU WANT TO CONNECT THEM CLOSE TO THE DEVICES.
VCSEL BACK CONTACT
3704
3702

Fig. 37

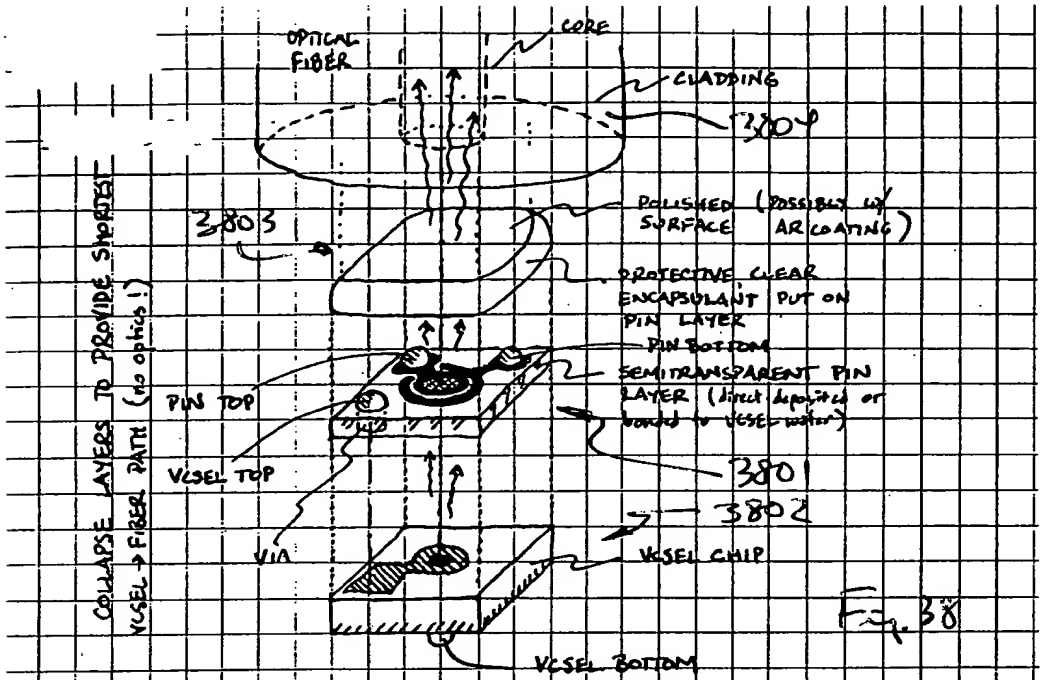


Fig. 38

.. SUCH A PACKAGE WOULD ALLOW LOW-COST, DIRECT COUPLING IN A FIBER CONNECTOR (VCSEL APERTURE < 25 μm AND MULTIMODE FIBER CORE ≈ 50-62.5 μm; VCSEL BEAM DIVERGENCE ≤ 20°, AND PIN LAYER IS THIN).

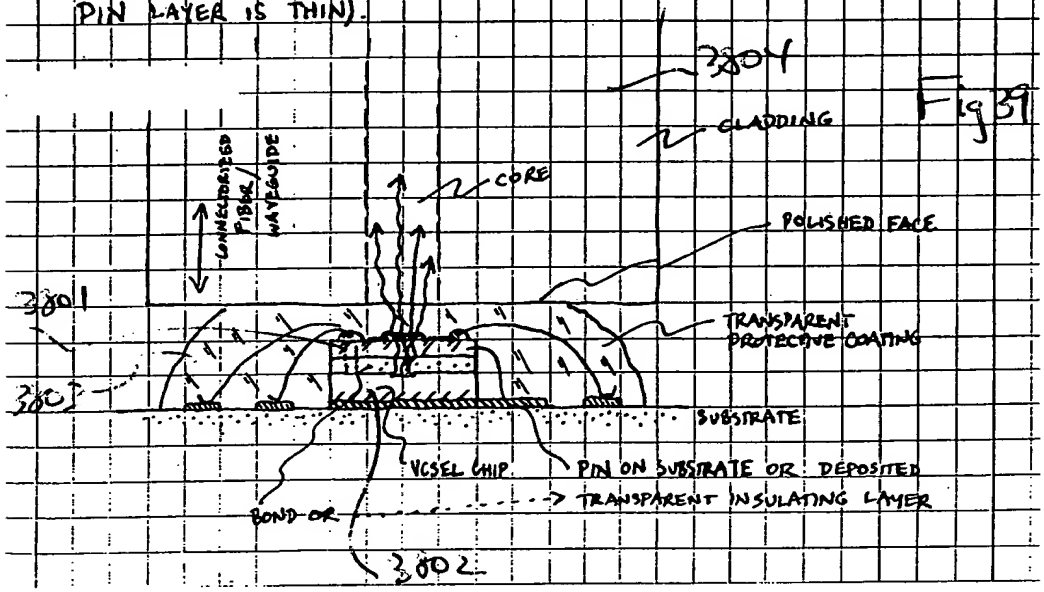
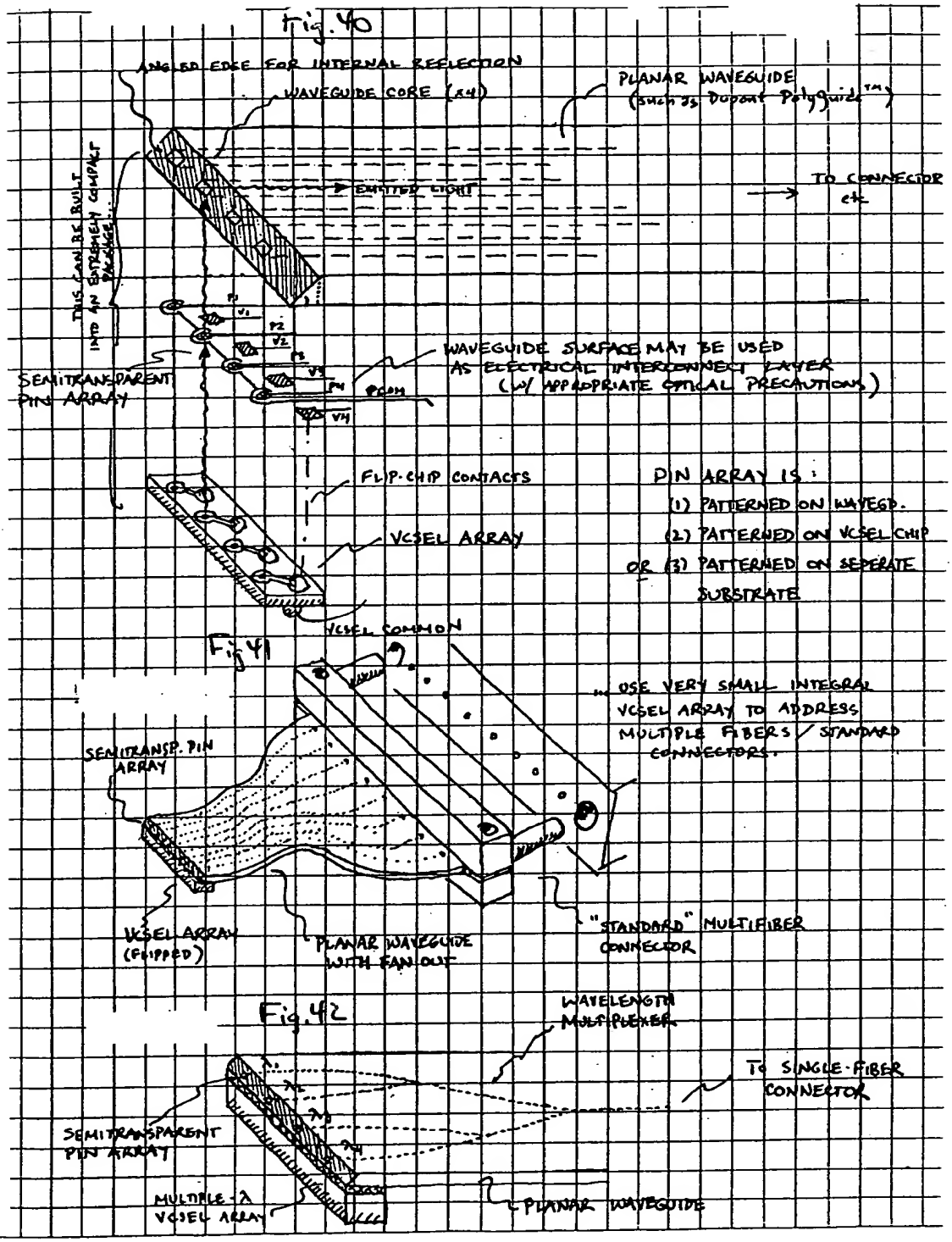


Fig 39

Fig. 40


ANGLED EDGE FOR INTERNAL REFLECTION
WAVEGUIDE CORE (n4)
PLANAR WAVEGUIDE (such as Dupont Polyguide™)
EMITTED LIGHT
TO CONNECTOR etc
THIS CAN BE BUILT INTO AN ENTIRELY COMPLETE PACKAGE
SEMITRANSPARENT PIN ARRAY
WAVEGUIDE SURFACE MAY BE USED AS ELECTRICAL INTERCONNECT LAYER (w/ APPROPRIATE OPTICAL PRECAUTIONS)
FLIP-CHIP CONTACTS
VCSEL ARRAY
PIN ARRAY IS:
(1) PATTERNED ON WAVEGD.
(2) PATTERNED ON VCSEL CHIP
OR (3) PATTERNED ON SEPERATE SUBSTRATE
VCSEL COMMON
Fig 41
... USE VERY SMALL INTEGRAL VCSEL ARRAY TO ADDRESS MULTIPLE FIBERS / STANDARD CONNECTORS.
SEMITRANSP. PIN ARRAY
VCSEL ARRAY (FLIPPED)
PLANAR WAVEGUIDE WITH FAN OUT
"STANDARD" MULTIFIBER CONNECTOR
Fig. 42
WAVELENGTH MULTIPLEXER
TO SINGLE-FIBER CONNECTOR
SEMITRANSPARENT PIN ARRAY
MULTIPLE-λ VCSEL ARRAY
PLANAR WAVEGUIDE